Webology (ISSN: 1735-188X)
Volume 18, Number 6, 2021

Implementation And Power Quality Analysis Of Half Bride Modular Multi-Level Inverter Using Nearest Level Modulation Technique Up To 22 Levels

Jahangeer Badar Soomro[1] , Faheem A. Chachar[1] , Farah Shah[1] , Jamshed Ahmed Ansari[1] , Sadaqat Ali [1] , Afaque Manzoor Soomro[1]

[1]Department of Electrical Engineering, Sukkur IBA University, Sindh, Pakistan.

Abstract- Modular Multilevel inverters have now become need for most of the modern applications like HVDC systems, Electric vehicles, Variable speed drives and Flexible Alternating-current Transmission system (FACTS) because of their better power quality and lesser total harmonic distortion as compared to other inverters. Many PWM techniques are used to power these converters. The existing techniques are reason for greater switching losses. This paper provides a practical criteria for the choice of modulation technique for MMCs. Also, there is an attempt to implement MMC up to 22 levels by using nearest level modulation technique which is considered to be simpler and robust for the systems like MMC, and these levels are then compared in terms of THD produced by each level.

Keywords- Modular Multilevel Converter (MMC), Nearest level Modulation (NLM), Total Harmonic distortion (THD).

I- Introduction

Inverter is a power electronic converter that converts DC power supply to an AC waveform. They are usually used in solar panels and other sort of these devices in order to use that DC power into powering some useful AC loads. The output that is produced depends upon the type of inverter that we are using. It can be square wave, quasi square wave or sine wave inverter. Even if we are using sine wave inverter, the output that is produced is not purely sinusoidal as it contains some harmonics. These harmonics are the component of periodic wave that are multiple of the fundamental frequency and produce distortion in the output. These harmonic distortions can be minimized by using a suitable modulation technique or by using a suitable converter topology.

Modular multilevel converters can have high number of levels with greater efficiency and lesser harmonic distortions [2]. They have the capability to manage high voltage operation without series-connecting switching devices. They provide lower common mode voltages and higher power quality. They offer high modularity, scalability, transformer less operation, lesser switching losses and lower filtering cost [1].

II- Modular Multilevel Converters

Modular multilevel converter consists of arms i.e. upper arm and lower arm. Each arm has submodules (SM), each connected in series [2]. The upper arm and lower arm are connected to an inductor and resister in order to limit fault current due to voltage difference in the arms. Capacitor is inserted in each submodule while each submodule consists of a half bridge circuit in order to get a particular voltage level. Also each switch has a diode in parallel in order to control the current flow. The working principle and the generation output levels of MMC can be understood by applying KVL to the basic structure of the circuit as shown in figure 1. Here Vdc is the supplied DC voltage, Vm(1-4) is the voltage across submodules and Vo is the output voltage. By neglecting the arm inductance and assuming the capacitors as DC sources, KVL is applied on the upper and lower arm.

For upper arm:

$$\mathbf{Vo} = \frac{\mathbf{Vdc}}{\mathbf{2}} - \mathbf{Vm1} - \mathbf{Vm2}$$

For lower arm:

$$\mathbf{Vo} = -\frac{\mathbf{Vdc}}{\mathbf{2}} + \mathbf{Vm3} + \mathbf{Vm4}$$

The potential of Vo = Vdc/2 can be achieved by bypassing the two modules at the upper top and connecting both modules in the lower loop. The potential of Vo= -Vdc/2 can be achieved by connecting both the upper modules and bypassing the two lower modules.[4] Similarly, in order to achieve zero level bypass one module from both the upper and lower loops. This can be achieved by 4 different ways. In this way the output voltage levels are generated corresponding to each loop.

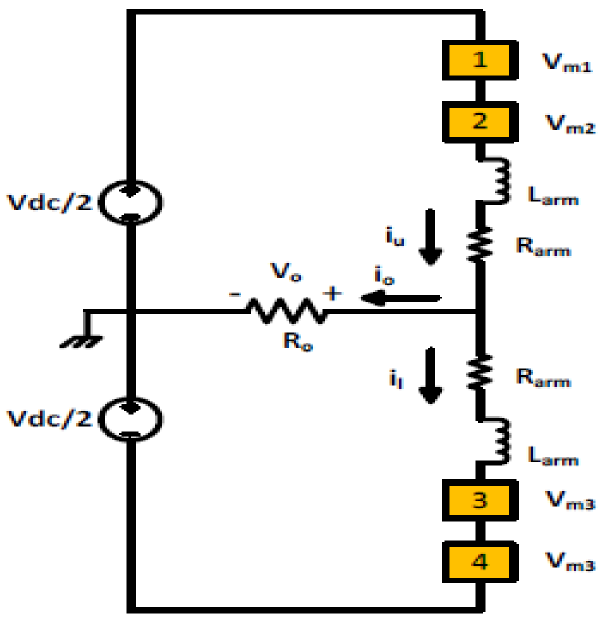

Figure 1: Basic Structure of MMC

The submodule operation has 3 operating states:

- Blocking State
- Cut-inn State
- Cut-off State

The summarized operation of all the operating states is shown in the table 1 below:

Table 1: Summary of the operation of Submodules

States	SM1	SM2	D1	D2	Capacitor
Blocking State	OFF	OFF	ON OFF	OFF ON	Inserted Not Inserted
Cut-in State	ON	OFF	-	-	Inserted
Cut-off State	OFF	ON	-	-	Not Inserted

So the overall topology of the circuit used is shown in figure 2.

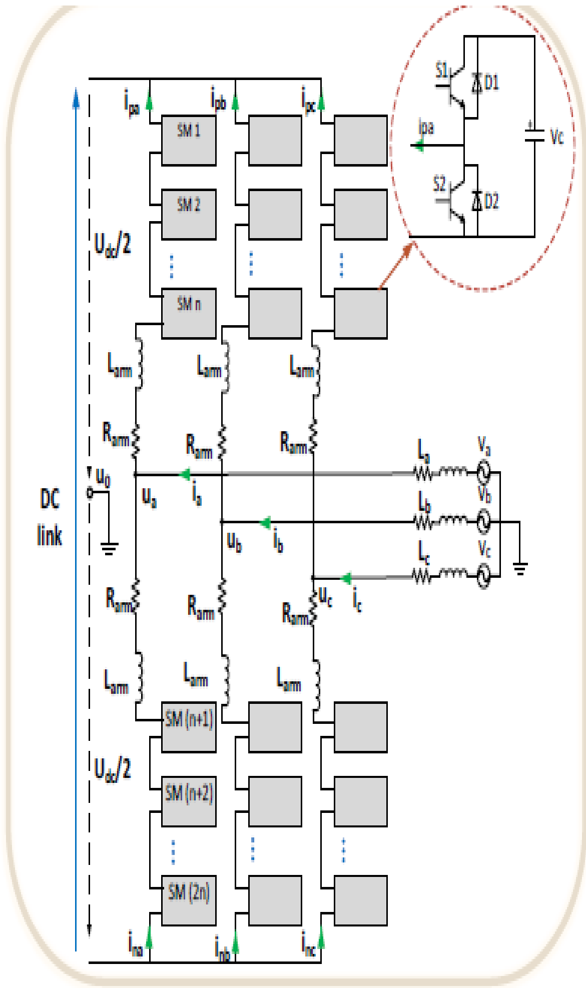

Figure 2: Circuit topology

III- Modulation Technique

Modulation technique used to power MMC plays a vital role in its proper working and efficiency. By using different PWM techniques the levels of output can vary as per our desired requirement and application [5]. Sinusoidal PWM techniques are the most common PWM techniques used and they are further classified into Level Shifted and Phase Shifted PWM techniques. Other variations of level shifted PWM techniques include In Phase Deposition (IPD), Phase Opposite Deposition (POD) and Alternate Phase Opposite Deposition (APOD). These techniques use a sine wave and different triangular waves, they are then compared in order to generate different levels of output voltages [7]. As there are number of waves compared so this contributes to more switching losses.

Nearest level modulation technique (NLM) is an alternative method for carrier-based modulation techniques that utilized more waves and increased the complexity [2] It has the advantage of being simple for implementation. It was introduced for mainly large-drive multilevel systems but it can also be used for MMC based HVDC applications as it is more flexible and provides easy digital implementation when the converter is operating at higher number of levels. It avoids the use of triangular carrier waves and directly computes the switching states and duty cycles [3]. The main idea behind is to sample the reference at frequency Fs and then approximate it to the nearest level resulting in natural fundamental switching frequency with reduced switching losses. For a MMC of N submodules per arm, NLM produces N+1 output voltage levels. Higher the frequency on which a converter operates on, better the approximation of the reference signal. Now the reference waveform becomes a staircase and the lower levels are used longer than the higher ones and hence this leads to the unbalance of capacitor voltage [9]. Therefore, NLM is not suitable for directly assigning to the submodules, instead it requires a sorting algorithm before it is fed to the converter in order to ensure submodule energy balance. Figure 3 shows the block diagram while figure 4 shows the working of NLM. The block diagram shows that at first the reference voltage is normalized with the capacitor voltage of the submodule in the gain block then the round function gives the closest integer number of the submodules to insert in order to approximate the reference voltage with the nearest voltage level [8]. Afterwards the sorting algorithm is applied as shown in figure 4 and 5.

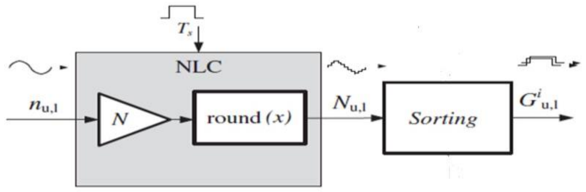

Figure 3: Nearest Level Control (NLC) Block Diagram

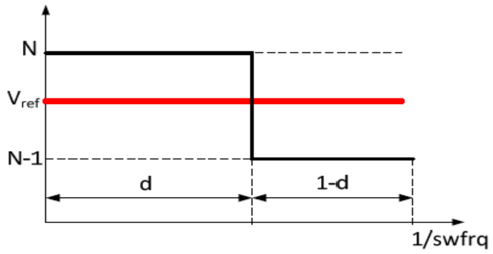

Figure 4: NLM working principle

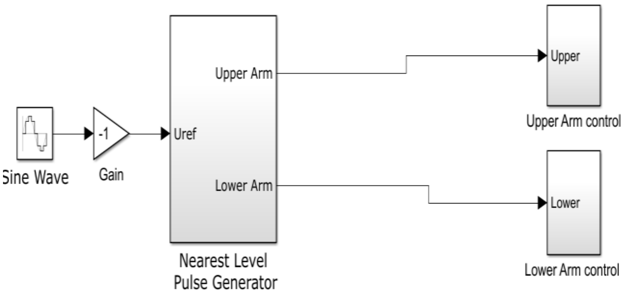

Figure 5: NLM feeding the upper and lower arm

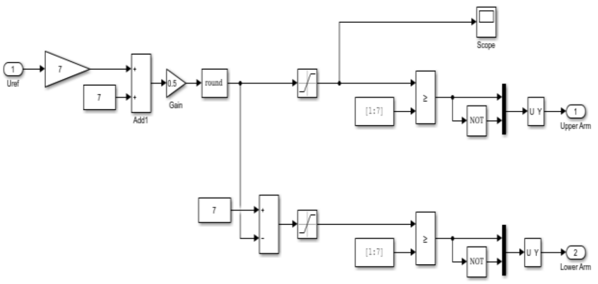

Figure 6: Sorting Algorithm Implemented in Simulink

IV- MATLAB/SIMULINK Simulation Model

The simulation model of MMC by using nearest level modulation technique is implemented in MATLAB/SIMULINK environment for 8, 11, 16 and 22 levels of the output voltage. For N number of submodules, N+1 levels are generated and each submodule consists of half bridge circuit. So for 8 levels, 7 submodules per arm are required and same is the case for achieving other levels. The output voltage levels are obtained in the presence of RL load. The parameter value of components used are: Capacitor=10F, Inductor=10mH, Resistive load=1ohm, Inductive load=10mH and Capacitor Voltage of Submodule=10 V.

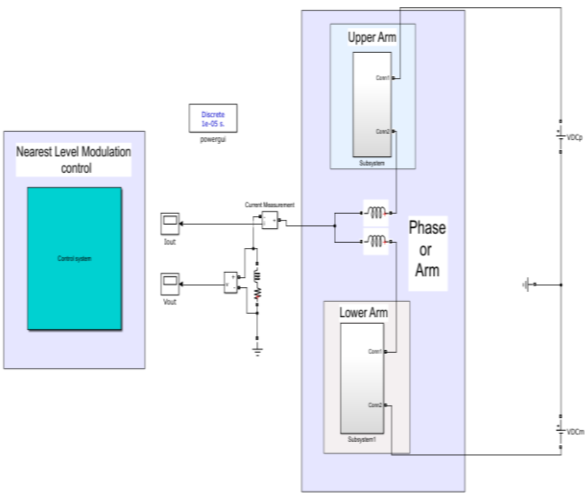

Figure 7: Simulation Model in Simulink

The output voltage, output current and calculation of THD for output voltage and current by using FFT analysis of the desired levels are given below:

A- For 8 Levels

For the implementation of 8 levels, 14 submodules (combined) are used in both the upper and lower arm. Each arm is fed with NLM technique and the output is observed for the levels of voltage and current and their respective THDs.

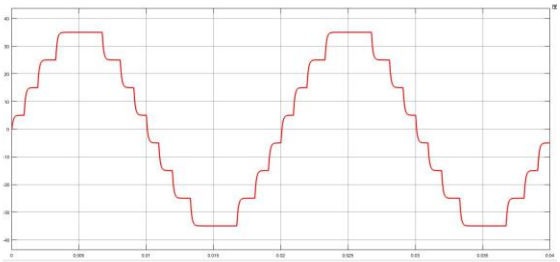

Figure 8: Output voltage for 8 levels

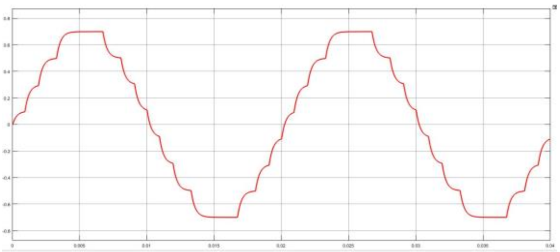

Figure 9: Output current for 8 levels

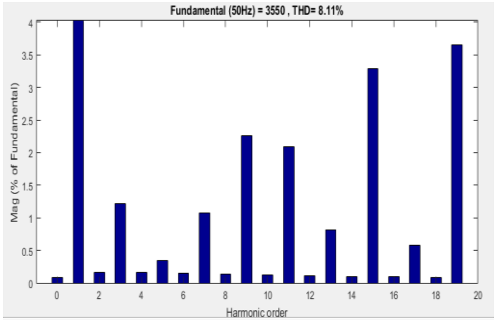

Figure 10: Voltage THD for 8 levels

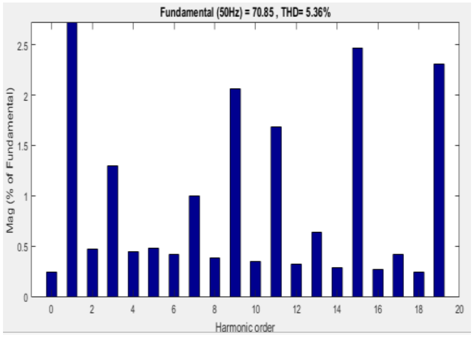

Figure 11: Current THD for 8 levels

B- For 11 levels

For the implementation of 11 levels, 20 submodules (combined) are used in both the upper and lower arm. Each arm is fed with NLM technique and the output is observed for the levels of voltage and current and their respective THDs.

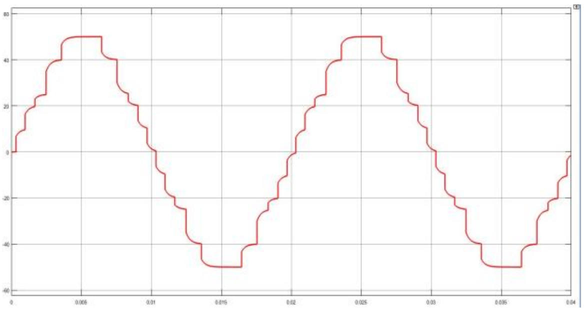

Figure 12: Output Voltage for 11 levels

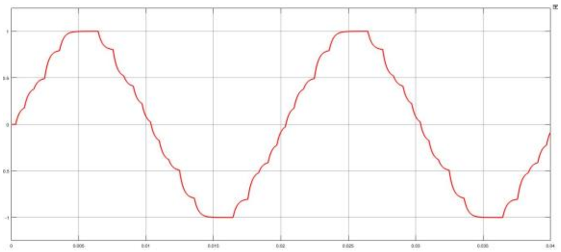

Figure 13: Output Current for 11 levels

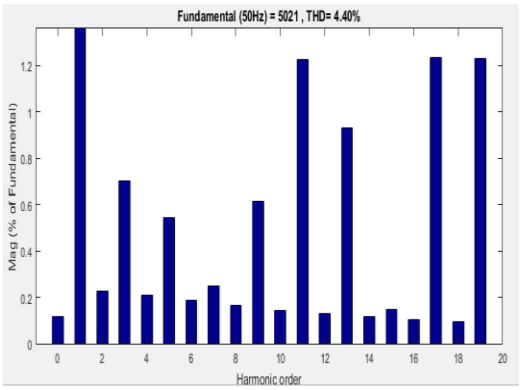

Figure 14: Voltage THD for 11 levels

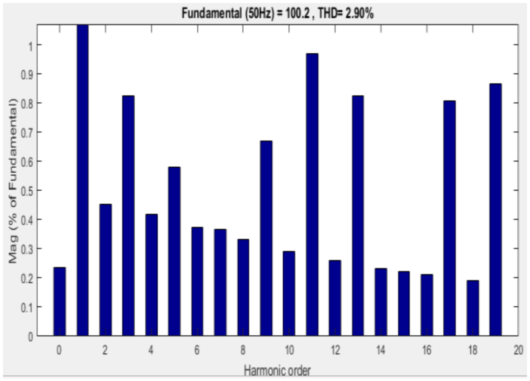

Figure 15: Current THD for 11 levels

C- For 16 levels

For the implementation of 16 levels, 30 submodules (combined) are used in both the upper and lower arm. Each arm is fed with NLM technique and the output is observed for the levels of voltage and current and their respective THDs.

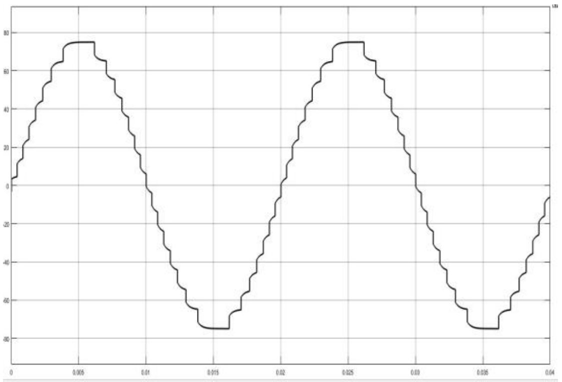

Figure 16: Output Voltage for 16 levels

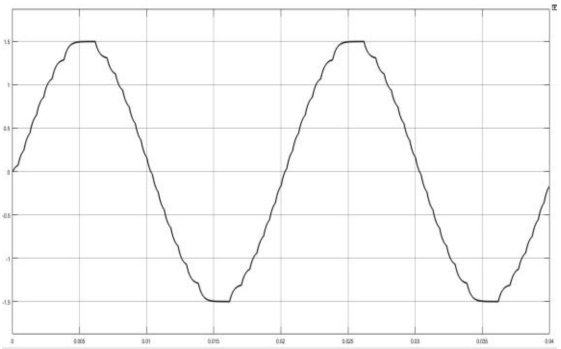

Figure 17: Output Current for 16 levels

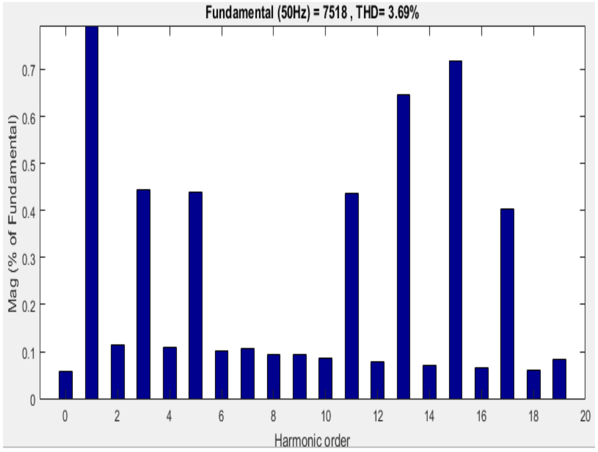

Figure 18: Voltage THD for 16 levels

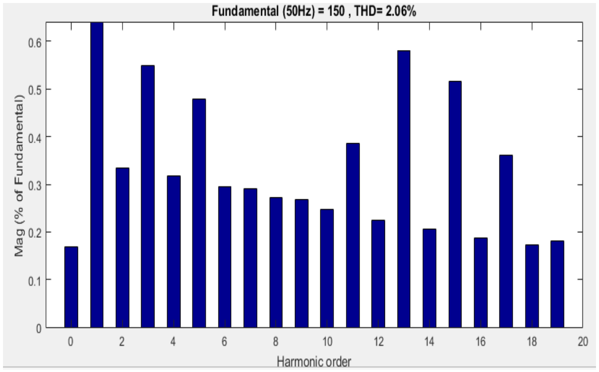

Figure 19: Current THD for 16 levels

D- For 22 levels

For the implementation of 22 levels, 42 submodules (combined) are used in both the upper and lower arm. Each arm is fed with NLM technique and the output is observed for the levels of voltage and current and their respective THDs.

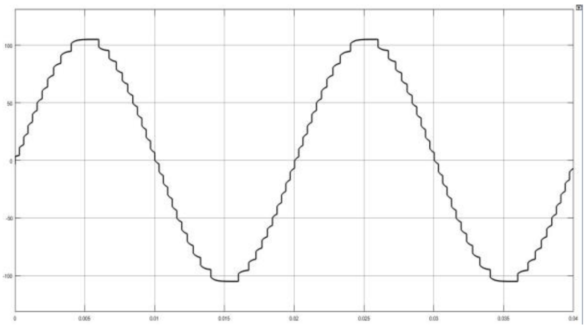

Figure 20: Output Voltage for 22 levels

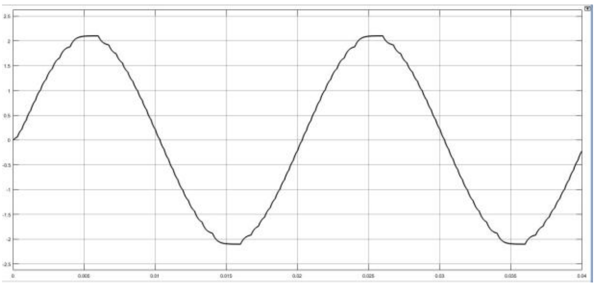

Figure 21: Output Current for 22 levels

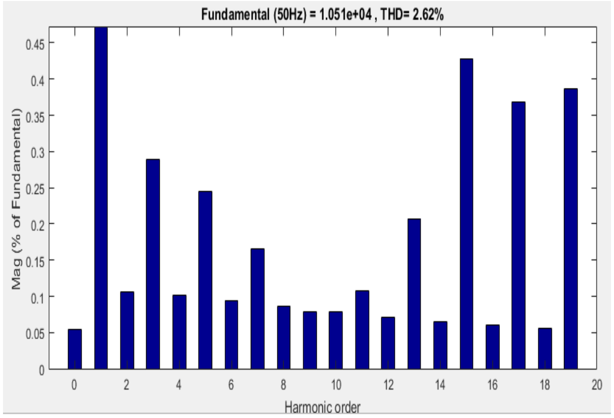

Figure 22: Voltage THD for 22 levels

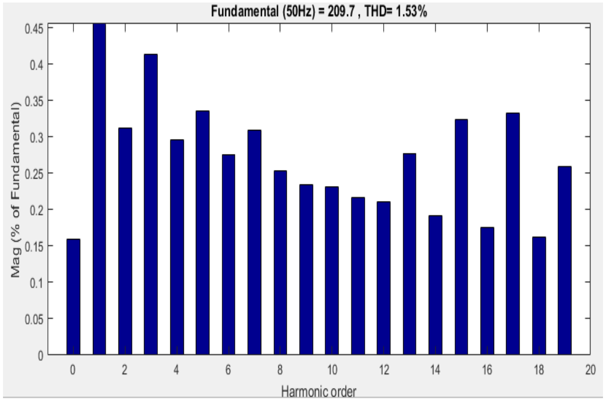

Figure 23: Current THD for 22 levels

V- Results

The simulation results are summarized in the tables below:

Table 2: Results for Output Voltage

Submodules	Levels	Voltage THD	Current THD
7	8	8.11%	5.36%
10	11	6.55%	5.24%
15	16	3.69%	2.06%
21	22	1.94%	1.53%

VI- Conclusion

The simulation results conclude that the MMC implemented by using nearest level modulation technique generates lesser THD as the number of levels increase. The THD level produced by this configuration is very much lesser than other topologies of multilevel inverters or by using other types of PWM techniques used for modulation.

REFERENCES

[1] Hu P, Jiang D. A level-increased nearest level modulation method for modular multilevel converters. IEEE transactions on Power Electronics. 2015 Apr;30(4):1836-42.

[2]

Guan M, Xu Z, Tu Q, Pan W. Nearest Level Modulation for Modular Multilevel Converters in HVDC Transmission [J]. Automation of Electric Power Systems. 2010 Jan;2:012.

[3] Wu D, Peng L. Characteristics of nearest level modulation method with circulating current control for modular multilevel converter. IET Power Electronics. 2016 Feb 10;9(2):155-64.

[4] Timofejevs A, Gamboa D, Liserre M, Teodorescu R, Chaudhary SK. Control of transformer less MMC-HVDC during asymmetric grid faults. In Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE 2013 Nov 10 (pp. 2016-2021). IEEE.

[5] Sharifabadi K, Harnefors L, Nee HP, Norrga S, Teodorescu R. Design, control, and application of modular multilevel converters for HVDC transmission systems. John Wiley & Sons; 2016 Oct 17.

[6] Moranchel M, Huerta F, Sanz I, Bueno E, Rodríguez FJ. A comparison of modulation techniques for modular multilevel converters. Energies. 2016 Dec 20;9(12):1091.

[7] Beddard A, Barnes M. Modelling of mmc-hvdc systems–an overview. Energy Procedia. 2015 Jan 1;80:201-12.

[8] Barnes M, Beddard A. Voltage source converter HVDC links–the state of the art and issues going forward. Energy Procedia. 2012 Jan 1;24:108-22.

[9] Asimakopoulos P. Design and Control of Modular Multilevel Converter in an Active Front and Application (Doctoral dissertation, CERN).

[10] Deng Y. Modulation, control, and applications of multilevel converters for power systems with high penetration of wind energy (Doctoral dissertation, Georgia Institute of Technology).

[11] Taylor J, Doerksen J, Filizadeh S. Design and Implementation of a Modular Multilevel Converter.

[12] Perez MA, Bernet S, Rodriguez J, Kouro S, Lizana R. Circuit topologies, modeling, control schemes, and applications of modular multilevel converters. IEEE transactions on power electronics. 2015 Jan;30(1):4-17.

[13] Friedrich K. Modern HVDC PLUS application of VSC in modular multilevel converter topology. In Industrial Electronics (ISIE), 2010 IEEE International Symposium on 2010 Jul 4 (pp. 3807-3810). IEEE.

[14] Tu Q, Xu Z. Impact of sampling frequency on harmonic distortion for modular multilevel converter. IEEE Transactions on Power Delivery. 2011 Jan;26(1):298-306.